IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:		PATENT APPLICATION
Inventors:	Jong-Jan Lee and Sheng Teng Hsu	
Serial No.:	Not Yet Assigned	Attorney Docket No. SLA 0696
Filed:	Herewith	
Title:	FABRICATION OF SILICON-ON-NOTHING (SON) MOSFET FABRICATION USING SELECTIVE ETCHING Si_{1-X} Ge_X LAYER	

Honorable Commissioner for Patents
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. §1.97

Sir:

Listed on attached Form PTO-1449 is information submitted pursuant to 37 C.F.R. §1.56. A copy of each listed publication is submitted herewith.

Applicant respectfully requests that the listed information be considered by the Examiner and made of record in the above-identified application.

(Date) 7/22/03

Respectfully submitted,

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1449A/PTO Rev. 10/95	U.S. Department of Commerce Patent and Trademark Office	Complete If Known	
LIST OF PRIOR ART CITED BY APPLICANT *(use as many sheets as necessary)*		Application Number	
		Filing Date	07-22-03
		First Named Inventor	Jong-Jan Lee
		Group Art Unit	
		Examiner Name	
Sheet 1 of 1		Attorney Docket No.	SLA.0696

U.S. PATENT DOCUMENTS

Examiner Initials	Cite No.[1]	U.S. Patent Document Kind Number	Code[2] (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YY	Pages, Columns, Lines, Where Relevant Passages or Figures Appear

FOREIGN PATENT DOCUMENTS

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OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, country where published, source.	T[2]
		M. JURCZAK *ET AL.*, *SON (Silicon on Nothing) - A New Device Architecture for the ULSI Era*, VLSI Tech. Dig., p.29, (1999).	
		R. KOH, *Buried Layer Engineering to Reduce the Drain-Induced Barrier Lowering of Sub-0.05um SOI-MOSFET* Jpn. J. Appl. Phys., Vol. 38, P. 2294 (1999)	
		M. JURCZAK, *ET AL.*, *Silicon-on-Nothing (SON) - an innovative Process for Advanced CMOS,* IEEE Trans. El. Dev. Vol. 47, pp2179-2187 (2000).	
		R. CHAU *ET AL.*, *A 50nm Depleted-Substrate CMOS Transistor*, IEDM, p. 621, 2001.	
		T. SATO *ET AL.*, *SON (Silicon on Nothing) MOSFET Using ESS (Empty Space in Silicon) Technique for SoC Application*, IEDM, p. 809, 2001.	

Examiner Signature		Date Considered	

Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.
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